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09/01/00 JC675 U.S. PTO

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PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42390.P4222D2 Total Pages 2

First Named Inventor or Application Identifier Robert S. Chau

Express Mail Label No. EL143556853US

JC564 U.S. PTO 09/654315 09/01/00

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 27)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 12)

4. X Oath or Declaration (Total Pages 6)
   a. ___ Newly Executed (Original or Copy)
   b. X Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. X Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. _ Microfiche Computer Program (Appendix)

7. _ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy

b. ____ Paper Copy (identical to computer copy)

c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))

9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

   ____ b. Power of Attorney

10. ____ English Translation Document (if applicable)

11. _X_ a. Information Disclosure Statement (IDS)/PTO-1449

    _X_ b. Copies of IDS Citations

12. _X_ Preliminary Amendment

13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. ____ a. Small Entity Statement(s)

    ____ b. Statement filed in prior application, Status still proper and desired

15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: ____________________

17. If a **CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

____ Continuation _X_ Divisional ____ Continuation-in-part (CIP)

of prior application No: **09/115,405 Filed July 14. 1998**

18. **Correspondence Address**

____ Customer Number or Bar Code Label ____________________

(Insert Customer No. or Attach Bar Code Label here)

or

X Correspondence Address Below

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FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT ($)846.00

Complete if Known:
Application No. Pending
Filing Date Herewith
First Named Inventor Robert S. Chau
Group Art Unit Pending
Examiner Name Pending
Attorney Docket No. 42390.P4222D2

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name ______

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

2. X **Payment Enclosed:**
   X **Check**
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FEE CALCULATION

1. **BASIC FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	$690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

Please enter the preliminary amendment prior to claim calculation.

2. **EXTRA CLAIM FEES**

			Extra Claims		Fee from below		Fee Paid
Total Claims	12	– 20** =	0	X		=	
Independent Claims	5	– 3** =	2	X	78.00	=	156.00
Multiple Dependent						=	

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 156.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	______
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	______
139	130	139	130	Non-English specification	______
147	2,520	147	2,520	For filing a request for reexamination	______
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	______
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	______
115	110	215	55	Extension for response within first month	______
116	380	216	190	Extension for response within second month	______
117	870	217	435	Extension for response within third month	______
118	1,360	218	680	Extension for response within fourth month	______
128	1,850	228	925	Extension for response within fifth month	______
119	300	219	150	Notice of Appeal	______
120	300	220	150	Filing a brief in support of an appeal	______
121	260	221	130	Request for oral hearing	______
138	1,510	138	1,510	Petition to institute a public use proceeding	______
140	110	240	55	Petition to revive unavoidably abandoned application	______
141	1,210	241	605	Petition to revive unintentionally abandoned application	______
142	1,210	242	605	Utility issue fee (or reissue)	______
143	430	243	215	Design issue fee	______
144	580	244	290	Plant issue fee	______
122	130	122	130	Petitions to the Commissioner	______
123	50	123	50	Petitions related to provisional applications	______
126	240	126	240	Submission of Information Disclosure Stmt	______
581	40	581	40	Recording each patent assignment per property (times number of properties)	______
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	______
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	______

Other fee (specify) ____________________ ______

Other fee (specify) ____________________ ______

SUBTOTAL (3) $ 0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Michael A. Bernadicou

Signature M. Bernadicou **Date** 8/24/00

Reg. Number Reg. No. 35,934 **Deposit Account User ID** ______
(complete if applicable)

Attorney's Docket No. 42390.P4222D2 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Robert S. Chau, et al.

U.S. Serial No: Pending

Filed: Herewith

For: Device Structure And Method For Reducing Silicide Encroachment

Which is a Divisional of Application

U.S. Serial No. 09/115,405

Filed: July 14, 1998

Examiner: Guerrero, M.

Art Unit: 2822

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

In the Divisional Application filed concurrently herewith, please enter this amendment and consider the following remarks.

"Express Mail" mailing label number: EL143556853US
Date of Deposit: September 1, 2000
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Cindy Murphy
(Typed or printed name of person mailing paper or fee)

Cindy Murphy
(Signature of person mailing paper or fee)

9/1/00
(Date signed)

IN THE SPECIFICATION

On page 2 line one please insert --This is a Divisional Application of Serial No. 09/115,405 filed on July 14, 1998 which is a Divisional Application of Serial No. 08/884,912 filed on June 30, 1997. --

IN THE CLAIMS:

Please cancel Claims 1-29 without prejudice.

Please add the following claims.

30. A semiconductor device comprising:

a gate electrode formed on a gate dielectric formed on a substrate surface, the gate electrode having a first thickness;

a gate silicon germanium film formed on the gate electrode, the gate silicon germanium film having a second thickness;

a gate silicide layer formed on the gate silicon germanium film, the silicide layer having a third thickness;

a pair of sidewall spacers on opposite sides of the gate electrode, the sidewall spacers having a first height above the substrate surface, the first height greater than the sum of the first and second and third thicknesses.

31. The semiconductor device of claim 30, wherein the gate electrode is polysilicon.

32. The semiconductor device of claim 30, further comprising:

a pair of source and drain regions formed on opposite sides of the gate electrode.

33. A semiconductor device comprising:

a pair of source/drain regions formed on opposite sides of a silicon gate electrode;

a silicon germanium film formed on the source/drain regions; and

a silicide layer formed on the silicon germanium film.

34. The semiconductor device of claim 33 further comprising:

an isolation region having a top surface positioned below the germanium film.

35. The semiconductor device of claim 33 further comprising:

an isolation region having a top surface positioned below the silicide layer.

36. A semiconductor device comprising:

a silicon gate electrode formed on a gate dielectric formed on a substrate surface, the silicon gate electrode having a first thickness;

a gate silicon germanium film formed on the silicon gate electrode, the gate silicon germanium film having a second thickness;

a gate silicide layer formed on the gate silicon germanium film, the gate silicide layer having a third thickness, the third thickness greater than the first thickness;

a pair of sidewall spacers on opposite sides of the silicon gate electrode, the sidewall spacers having a first height above the substrate surface, the first height greater that the sum of the first and second and third thicknesses;

a pair of source/drain regions formed on opposite sides of the silicon gate electrode;

a source/drain silicon germanium film formed on the source/drain regions; and

a source/drain silicide layer formed on the source/drain silicon germanium film.

37. The semiconductor device of claim 36 wherein the silicon gate electrode is polysilicon.

38. A method of forming a semiconductor device comprising:

forming a gate electrode having a first thickness on a gate dielectric layer formed on a first surface of a substrate;

forming a pair of source/drain regions on opposite sides of the gate electrode;

forming a silicon germanium film having a second thickness on the gate electrode;

forming a silicon germanium film having the second thickness on the source/drain regions;

forming a silicide layer having a third thickness on the silicon germanium films.

39. The method of claim 38 further comprising:

forming a pair of sidewall spacers having a first height above the substrate surface on opposite sides of the gate electrode, wherein the first height is greater than the sum of the first and second and third thicknesses.

40 . The method of claim 39, wherein the sidewall spacers comprise silicon nitride.

41. A method of forming a semiconductor device, comprising:

forming an isolation region having a top surface in a semiconductor substrate;

etching the semiconductor substrate adjacent to the isolation region to form a recess region;

depositing a silicon germanium film having a top surface in the recessed region; and

depositing a silicide layer having a top surface over the silicon germanium film.

42. The method of forming a semiconductor device of claim 41, wherein the silicide layer top surface extends above the isolation region top surface.

43. The method of forming a semiconductor device of claim 42, wherein the silicon germanium film top surface extends above the isolation region top surface.

REMARKS

This preliminary amendment is being filed in response to a restriction requirement given in a previous Divisional Application Serial No. 09/115,405 filed on July 14, 1998. Both the Parent Application, Serial No. 08/884,912 filed on June 30, 1997, and the previous Divisional Application Serial No. 09/115,405 are presently co-pending.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 9/1, 2000

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UNITED STATES PATENT APPLICATION

for

DEVICE STRUCTURE AND METHOD FOR REDUCING SILICIDE ENCROACHMENT

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Attorney Docket No.: 042390.P4222

EXPRESS MAIL MAILING CERTIFICATE

"Express Mail" mailing label number: EM389985911US

Date of Deposit: June 30, 1997

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Christine M. Gregovich

(Typed or printed name of person mailing paper or fee)

Christine M. Gregovich

(Signature of person mailing paper or fee)

June 30, 1997

(Date signed)

DEVICE STRUCTURE AND METHOD FOR REDUCING SILICIDE ENCROACHMENT

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to the field of semiconductor device fabrication, and more specifically to a method and structure for reducing silicide encroachment in an integrated circuit.

2. DISCUSSION OF RELATED ART

Today integrated circuits are made up of literally millions of active and passive devices such as transistors, capacitors, and resistors. In order to improve device performance, low resistance silicide layers are generally formed on electrodes such as gate electrodes and on doped regions such as source/drain regions.

For example, Figure 1A is an illustration of a portion of a complementary metal oxide semiconductor (CMOS) integrated circuit. Integrated circuit 100 includes a PMOS transistor 102 and an NMOS transistor 104 separated by an isolation region 103. NMOS and PMOS transistor 102 and 104 each include a pair of source/drain regions 106, a polysilicon gate electrode 107, and a gate dielectric layer 101. Insulative sidewall spacers 108 are formed along opposite sidewalls of gate electrode 107 as shown in Figure 1A. In order to decrease the resistance of gate electrode 107 and source/drain

regions 106, low resistance silicide is formed on gate electrode 107 and source/drain regions 106.

One method of forming a low resistance silicide is a self-aligned silicide process known as a SALICIDE process. In such a process, a refractory metal layer 109, such as titanium, tungsten, cobalt, nickel or palladium, is blanket deposited over the substrate and MOS devices 102 and 104 as shown in Figure 1B. The substrate is then heated to cause a reaction between metal layer 109 and exposed silicon surfaces such as source/drain regions 106 and gate electrode 107 to form a low resistance silicide 110 as shown in Figure 1C. Locations where no silicon is available for reaction, such as oxide spacers 108 and isolation region 103, metal layer 109 remains unreacted. Unreacted metal 109 can then be etched away leaving silicide only on source/drain regions 106 and on gate electrode 107 as shown in Figure 1D.

A problem with the above described process is that circuits fabricated with the process are vulnerable to short circuits due to silicide encroachment. That is, during the high temperature anneal used to form silicide layer 110 or during subsequent anneal steps, silicide can diffuse or spill over from polysilicon gate electrode 107 and source/drain regions 106 and form an undesired silicide bridge 112 over sidewall spacers 108 and cause shorting of gate electrode 107 to source/drain region 106. Silicide encroachment is further compounded by silicides, such as nickel silicide (NiSi), which experience silicide volume increases over the combined volume of the consumed silicon and metal layer. For example, the reaction of nickel and silicon creates a nickel silicide/polysilicon gate electrode layer having an approximately 18% volume increase over the silicon electrode shown in Figure 1A. As such is shown in Figure 1C to silicide 110 reaches above spacer 108.

Silicide encroachment can also cause short circuits between source/drain regions of adjacent devices which are separated by planar isolation regions. For example, as also shown in Figure 1E, as isolation regions are made more planar and made more compact (less than .4 microns wide), such as with shallow trench isolation (STI), silicide from adjacent transistor source/drain regions 106 can diffuse or spill over isolation region 103 and cause silicide shorts 114 between adjacent devices.

In order to help reduce the potential for silicide shorts between source/drain regions and gate electrodes, polysilicon layer 107 is formed thick, (i.e., greater than 2000Å), in order to ensure that silicide 110 has a large distance to bridge over spacers 108. Unfortunately, however, by increasing the thickness of polysilicon gate 107, the ion implantation technique used to dope gate electrode 107 (typically the source/drain implantation) is unable to drive dopants sufficiently deep into the electrode 107 to provide a uniformly doped low conductivity gate electrode. When the lower portion (portion near gate dielectric layer 101) of the gate electrode has no or reduced doping, the device has increased gate resistance which detrimentally affects the drive current. This non uniform gate electrode doping is commonly referred to as "*polysilicon depletion effects*".

Additionally, in order to prevent silicide encroachment, silicide layer 110 is generally kept thin (i.e., thinner than the thickness of the polysilicon gate electrode). It would be desirable to be able to form silicide layers which are thicker than the polysilicon layer so that lower resistance electrodes can be fabricated and device performance improved.

Thus, what is desired is a device structure and method of fabrication which reduces silicide encroachment as well as poly depletion effects.

SUMMARY OF THE INVENTION

In a first embodiment of the present invention, a semiconductor device having a novel spacer structure and its method of fabrication is described. According to the first embodiment a semiconductor device having an electrode with a first thickness is formed. A silicide layer having a second thickness is formed on the electrode. A sidewall spacer formed adjacent to the electrode and has a height which is greater than the sum of the thickness of the electrode and the thickness of the silicide layer. In another embodiment of the present invention, regions of a device which are to receive silicide are etched below the top surface of isolation regions prior to silicide deposition. In this way silicide regions are formed below the top surface of the isolation regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is an illustration of a cross-sectional view of a conventional CMOS integrated circuit.

Figure 1B is an illustration of a cross-sectional view showing the formation of a metal layer over the substrate at Figure 1A.

Figure 1C is an illustration of a cross-sectional view showing the formation of a silicide layer from the metal layer on the substrate at Figure 1B.

Figure 1D is an illustration of a cross-sectional view showing the removal of unreacted metal from the substrate of Figure 1C.

Figure 1E is an illustration of a cross-sectional view showing silicide encroachment on the substrate of Figure 1D.

Figure 2 is an illustration of a cross-sectional view of a semiconductor substrate having silicide regions formed in accordance with the present invention.

Figure 3A is an illustration of a cross-sectional view showing the formation of a isolation region in a semiconductor substrate.

Figure 3B is an illustration of a cross-sectional view showing the formation of *p type* and *n* type conductivity regions in a semiconductor substrate.

Figure 3C is an illustration of a cross-section view showing the formation of a gate dielectric layer, a polysilicon layer, and a sacrificial layer on the substrate of Figure 3B.

Figure 3D is an illustration of a cross-sectional view showing the formation of an intermediate gate electrode on the substrate of Figure 3C.

Figure 3E is an illustration of a cross-sectional view showing the formation of sidewall spacers on the substrate of Figure 3D.

Figure 3F is an illustration of a cross-sectional view showing the formation of recesses and source/drain regions in the substrate of Figure 3E.

Figure 3G is an illustration of a cross-section view showing the removal of the sacrificial layer from the substrate of Figure 3F.

Figure 3H is an illustration of a cross-sectional view showing the formation of a metal layer over the substrate of Figure 3G.

Figure 3I is an illustration of a cross-sectional view showing the formation of silicide regions.

Figure 4A is an illustration of a cross-sectional view showing the formation of semiconductor material onto a semiconductor substrate.

Figure 4B is an illustration of a cross-sectional view showing the formation of silicide on the substrate of Figure 4A.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

A novel device structure and method for preventing silicide encroachment is described. In the following description numerous specific details are set forth such as specific materials and processes in order to provide a thorough understanding of the present invention. In other instances well known semiconductor processing techniques and machinery have not been set forth in detail in order to not unnecessarily obscure the present invention.

The present invention is a novel device structure and method for preventing silicide encroachment in an integrated circuit. In one embodiment of the present invention a sidewall spacer is formed adjacent to an electrode of a device onto which a silicide layer is to be formed. The spacer is fabricated so that it has a height which is greater than the combined thickness or height of the electrode plus the silicide layer. In this way the spacer extends above the height of the silicided electrode and prevents silicide from expanding or diffusing from the electrode and causing shorts with adjacent devices or regions.

In another embodiment of the present invention where isolation regions are used to isolate adjacent devices, devices are fabricated in such a manner that the isolation region extends above the silicided regions. According to this embodiment of the present invention, regions which are to receive silicide are etched below the top surface of the isolation region prior to silicide deposition. In this way, silicide is unable to expand or diffuse over the isolation region and cause electrical coupling or shorts between adjacent devices.

An example of an integrated circuit 200 which incorporates the structures and methods of the present invention is illustrated in Figure 2. Integrated circuit 200 includes a first metal oxide semiconductor device 202 and a second metal oxide semiconductor device 206 separated by an isolation region 204. Each MOS device includes a gate electrode 208 formed on a gate dielectric layer 210 which is formed on a first surface 212 of a substrate 214. Each gate electrode has a silicide layer 216 formed thereon. Semiconductor devices 202 and 206 each also include a pair of sidewall spacers 218 formed adjacent to and along opposite sides of the silicided gate electrodes 220 as shown in Figure 2. Sidewall spacers 218 extend a spacer height (T_{SP}) above substrate surface 212. Spacers 218 have a height (T_{SP})which is greater than the height (T_{Sg}) which the silicided gate electrode 220 extends above substrate surface 212 (i.e., $T_{SP} > T_{Sg}$). That is, spacer height (T_{SP}) is greater than the sum total of the gate electrode 208 thickness (T_g) and the silicide 216 thickness (T_S) (i.e., $T_{SP} > T_g + T_S$). Spacers 218 preferably extend at least 200Å above silicided gate electrode 220. Additionally, in an embodiment of the present invention, silicide layer 216 can be made much thicker, more than two times thicker, than the gate electrode 208. (i.e., $T_S > T_g$) In this way gate electrode resistance is substantially reduced and poly depletion effects eliminated.

In another embodiment of the present invention, integrated circuit 200 utilizes planar isolation regions 204, such as, shallow trench isolation (STI) , as shown in Figure 2. A planar isolation region 204 is characterized by the fact that the top surface 221 of isolation region 204 is substantially planar with substrate surface 212 on which gate dielectric layers 210 are formed. That is, the top surface 221 of isolation region 204 extends less than 1500Å above substrate surface 212. Shallow trench isolation regions are desirable because they can be formed planar and compact which dramatically improves device

packing density. In the embodiment of the present invention where planar isolation regions (e.g., STI) are utilized, source/drain regions 222 are etched or recessed prior to depositing silicide 224 on to the source/drain regions. In this way, the top surface 221 of isolation region 204 extends above the top surface 226 of silicide regions 224. In this way silicide is confined to the source/drain regions and is prevented from diffusing or expanding over the isolation region 204 and causing short circuits between the source/drain regions 224 of adjacent devices 202 and 206.

An example of a method of fabricating an integrated circuit according to methods of the present invention will be described with respect to the fabrication of a CMOS integrated circuit. The example describes a method of preventing silicide encroachment and thereby preventing shorts between a source/drain region and a gate electrode when forming a silicide on the gate electrode. Additionally the present example illustrates a method of preventing silicide encroachment between source/drain regions of adjacent transistors separated by a planar isolation region. The methods described herein can be used independently or integrated together to reduce or eliminate reliability issues associated with silicide encroachment. It is to be appreciated that the illustrated method of preventing silicide encroachment on a gate electrode is equally applicable to forming silicide layers on other electrodes such as but not limited to emitter electrodes of bipolar transistors and capacitor electrodes of DRAM cells. Similarly the illustrated method of preventing silicide encroachment between source/drain regions of adjacent transistors is equally applicable to preventing silicide encroachment over any isolation region separating other device regions such as base and collector contact regions and burried interconnects. The isolation process is especially useful when planar, compact isolation regions are used.

According to the present invention a substrate 300, such as shown in Figure 3A, is provided. Substrate 300 is generally a semiconductor substrate such as but not limited to a silicon substrate, a gallium arsenide substrate, a silicon germanium substrate, or a silicon on insulator (SOI) substrate. Additionally substrate 300 may or may not include additional epitaxial layers deposited thereon. Still further substrate need not necessarily be semiconductor substrate and can be other types of substrates such as those used for flat panel displays. For the purposes of the present invention a substrate is defined as a starting material on which devices of the present invention are fabricated.

According to an embodiment of the present invention, an isolation region 302 is formed on substrate 300. In order to fabricate high density integrated circuits, isolation region 302 is preferably a planar isolation region such as a shallow trench isolation (STI). An STI region 302 can be fabricated by a well known technique such as by blanket depositing a pad oxide layer 304 of about 100Å onto surface 301 of substrate 300 and a nitride layer 306 of about 1000Å onto pad oxide layer 304. Using standard photolithography and etching techniques, an opening can be formed through pad oxide layer 304 and silicon nitride layer 306 at locations where isolation regions are desired. Substrate 300 is then etched to form a trench in substrate 300 with well known techniques. Next, a thin (approximately 100-300Å) thermal oxide is grown within the trench. A fill material, such as silicon dioxide deposited by chemical vapor deposition (CVD), is then blanket deposited over silicon nitride layer 306 and into the trench. The fill material can then be polished back with chemical mechanical polishing until the top surface 312 of isolation region 302 is substantially planar with silicon nitride layer 306 as shown in Figure 3A.

Next, as shown in Figure 3B, silicon nitride layer 306 and pad oxide layer 304 are removed with well known techniques to form a shallow and compact isolation region 302. Isolation region 302 is said to be a planar isolation region when the top surface 312 of isolation region 302 has a height (T_{iso}) which is less than 1500Å above substrate surface 301. Additionally with the technique described above compact isolation regions having a width of less than .4 microns can be fabricated. It is to be appreciated that the use of small and planar isolation regions enables the fabrication of high density integrated circuits. Although STI regions are preferred, other types of planar isolation regions, such as recessed LOCOS and deep trench isolation may be utilized as well as non planar isolation regions, such as LOCOS isolation, if desired.

Next, as also shown in Figure 3B, well known masking and ion implementation techniques are used to form a *p* type region 314 and an *n* type region 316 in substrate 300.

Next, as illustrated in Figure 3C, a thin, less than 100Å, gate dielectric layer 318 such as but not limited to silicon dioxide, silicon nitride or silicon oxinitride is formed on surface 301 of substrate 300. A silicon film 320 is then deposited over gate dielectric layer 318 as shown in Figure 3C. Silicon film 320 is generally polycrystalline silicon but may be other forms of silicon such as amorphous silicon. Polysilicon layer 320 can be planarized at this time by chemical-mechanical polishing. In order to reduce polysilicon depletion effects as well as improve photolithography and etch processes, polysilicon layer 320 is formed as thin as possible. However, polysilicon layer 320 must be formed thick enough to prevent channel doping during subsequent source/drain doping. A planarized polysilicon layer having a thickness (T_g) of between 100-1500Å over substrate surface 301 is suitable. (It is to be noted

that gate thickness Tg over substrate surface 301 includes the nominal thickness of gate dielectric layer 318).

Next, as also shown in Figure 3C, a sacrificial layer 322 is deposited over polysilicon layer 320. Sacrificial layer 320 can be any suitable material which can be selectively etched with respect to subsequently formed spacers and polysilicon layer 320. Sacrificial layer 320 can be for example, a grown or CVD deposited oxide layer, a fluorine, phosphorous, or boron doped oxide layer, formed by any well known technique. Additionally sacrificial layer 320 can be a silicon/germanium semiconductor alloy. A silicon/germanium semiconductor alloy can be formed by a decomposition of SiH_2Cl_2 and GeH_4 in H_2 ambient at a temperature between 500-800°C with 600°C being preferred. It is to be appreciated that the thickness of sacrificial layer 322 sets the upper limit on the amount of silicide that can be subsequently formed on polysilicon layer 320. Sacrificial layer 322 is preferably made thicker than polysilicon layer 320 and ideally at least twice as thick. In this way the electrode can have a silicide layer which is thicker than the polysilicon layer which will allow for the formation of a low resistance electrode.

Next, as shown in Figure 3D, sacrificial layer 322, polysilicon layer 320 and gate dielectric layer 318 are patterned with well known photolithography and etching techniques to form intermediate electrodes 324. At this time if desired, tip regions or lightly doped regions can be formed. For example, well known photolithography and ion implantation techniques can be used to form *n* type conductivity tip regions 326 in *p* type conductivity region 314 and *p* type conductivity tip regions 328 and *n* type conductivity region 316 in alignment with the outside edges of intermediate gate electrodes 324, as shown in Figure 3D.

Next, a pair of sidewall spacers 330 are formed along opposite sides of intermediate gate electrode 324 as shown in Figure 3E. Sidewall spacers 330 can be formed by any well known method such as by blanket depositing a 100-1000Å thick conformal layer of silicon nitride over substrate 300 and then anisotropically etching the film to form sidewall spacers 330. Sidewall spacers 330 should be formed of a material which can be selectively etched with respect to sacrificial layer 322. Sidewall spacers 330 need not necessarily be single material spacers and can be composite spacers such as silicon nitride spacers with a thin oxide layer formed adjacent to the intermediate gate electrode 324. Sidewall spacers 330 have a height (T_{sp}) over substrate surface 301 which is equal to the combined thickness of polysilicon layer 320 (T_g) and sacrificial layer 322 (T_{sac}).

Next, if desired, substrate 300 can be etched in alignment with sidewall spacers 330 to form recesses 332 as illustrated in Figure 3F. Recesses 332 are desirable when planar isolation regions 302 are used to isolate source/drain regions of adjacent devices. Recesses 332 can also be used when non planar isolation regions are used in order to provide increased margins for preventing silicide encroachment over the isolation region. Recesses 332 are formed to a depth beneath surface 301 sufficient to keep subsequently formed silicide beneath the top surface of isolation region 302. Recesses having a depth beneath surface 301 of between 100-1000Å will generally be sufficient. Recesses 332 can be formed by any well known technique such as but not limited to reactive ion etching (RIE) with the chemistry comprising C_2H_6 and He at a ratio of 2:1. If a suitable spacer material is used, such as silicon nitride, recesses 322 can be formed by over etching into the silicon substrate 300 during the spacer etch.

Next, as illustrated in Figure 3G, sacrificial layer 322 is removed from polysilicon layer 320. If sacrificial layer 322 is an oxide, it can be removed with a diluted HF solution (50:1 H_2O to HF). If sacrificial layer 322 is silicon germanium it can be removed with a mixture of NH_4OH/H_2O_2 or sulfuric acid (H_2S0_4). Using a silicon germanium sacrificial layer 322 is advantageous because silicon germanium can be removed with an etchant which does not attack oxides which are generally used to fill STI region 302.

After sacrificial layer 322 has been removed, n type conductivity source/drain regions 331 and *p* type conductivity source/drain regions 333 can be formed as shown in Figure 3G. *N* type source/drain regions 331 and *p* type source/drain regions 333 can be formed by well known photolithography and ion implementation techniques. If polysilicon layer 320 is made as thin as practically possible, (i.e., less than 1000Å) the respective source/drain dopings will be able to dope the entire thickness of polysilicon layer 320, and thereby prevent polysilicon depletion effects. Additionally, by having a thin polysilicon layer, low energy (less than 30 Kev) source/drain implant energies can be used to form shallow source/drain junctions, and still ensure complete polysilicon doping. It is to be noted, that if desired deep source/drain regions 331 and 333 can be formed directly after spacer formation in Figure 3E. Recesses 332 can then be subsequently etched into the source/drain regions 331 and 333.

Next, a silicide layer is formed on polysilicon layer 320 and on source/drain regions 331 and 333. In one embodiment of the present invention the silicide layers are formed with a self-aligned silicide process or SALICIDE process. In a salicide process, a metal layer 334 is blanket deposited over substrate 300 as illustrated in Figure 3H. Metal layer 334 is generally a refractory metal such as but not limited to, titanium, tungsten, nickel, cobalt

and palladium which can react with silicon to form a low resistance silicide. Metal layer 334 can be deposited by any well known technique such as by sputtering.

Substrate 300 is now annealed (heated) to cause a chemical reaction between those portions of metal layer 334 which are in direct contact with exposed silicon to form a silicide. That is, silicide is formed wherever silicon is available to react with metal layer 334 such as over source/drain regions 331 and 333 and on polysilicon gate electrode 320. Since no silicon is available from sidewall spacers 330 or on STI region 302 no silicide forms thereon. Substrate 300 is heated to a sufficient temperature and for a sufficient period of time in order to initiate the reaction and produce low resistance silicide. Substrate 300 can be thermally cycled with well known techniques such as a rapid thermal anneal or a furnace anneal. Next, substrate 300 is subjected to a etchant which selectively removes the unreactive portions of metal layer 334 while leaving silicide 336 on polysilicon layer 320 and on source/drain regions 331 and 333.

It is to be appreciated that for preventing silicide encroachment on gate electrode 320, metal layer 334 is deposited to a thickness so that after the silicide reaction, spacers 330 extend above the formed silicide 336 and thereby confine the silicide layer between spacers 330. That is, metal layer 334 is deposited to a thickness so that after silicide formation the spacer height T_{sp} is greater than the sum of a polysilicon gate thickness (T_g) plus the silicide thickness (T_s), (i.e., $T_{sp} > T_g + T_s$). Similarly, for preventing silicide encroachment over isolation region 302, metal layer 334 is deposited to a thickness so that after silicide reaction silicide layer 336 on source/drain regions 331 and 333 are beneath the top surface of isolation region 302. That is, silicide 336 on source/drain regions 331 and 333 has a height less than T_{iso}

over substrate surface 301. In this way silicide 336 is confined to the source/drain regions 331 and 333 between spacers 330 and isolation region 302.

It is to be appreciated that when volume expanding silicides are utilized, such as nickel silicide, additional margin should be provided to ensure that the silicide is unable to expand over spacers 330 and/or isolation region 302. The confining techniques of the present invention enable the use of volume expanding silicide layers without worrying about silicide encroachment problems associated with the prior art.

In an alternative to forming silicide 336 by a self-aligned process, silicide layer 336 can be selectively deposited onto source/drain regions 331 and 333 and polysilicon layer 320. For example, titanium silicide can be selectively deposited onto source/drain regions 331 and 333 and gate electrode 320 by chemical vapor deposition (CVD) using reactive gasses comprising $TiCl_4$, SiH_2Cl_2, and/or SiH_4 with a hydrogen carrier gas at a temperature ranging from 600-900°C and a pressure between 5-100 torr. Such a process is said to be a selective process because it will form silicide only on exposed silicon surfaces, such as source/drain regions 331 and 332 and polysilicon gate electrode 320 and not on insulative regions such as spacers 330 or STI isolation region 302. It is recommended to utilize an HF dip prior to selective silicide deposition to ensure complete removal of all native oxide layers formed on silicon surfaces. A subsequent high temperature rapid thermal anneal can be used to convert the as deposited titanium silicide phase (C49) into low resistance phase (C54).

In a selective deposition process, insignificant amounts of silicon are consumed during the deposition as compared to a salicide process. Since less silicon is needed to support the silicide deposition, when a selective silicide

process is used polysilicon layer 320 can be formed very thin to further decrease poly depletion effects and improve photolithography and etching processes.

It is to be appreciated that it may be desirable to selectively deposit semiconductor material prior to silicide formation. For example, after forming sidewall spacers 330 and recesses 332, and removing sacrificial layer 322 it may be desirable to selectively deposit a semiconductor material, such as silicon germanium, into recesses 332 and onto polysilicon layer 320 as shown in Figure 4A. Ion implementation or insitu doping, can be used to dope the semiconductor material to the desired conductivity type and concentration. Additionally, a subsequent anneal step can be used to out diffuse dopants from the semiconductor material to form ultra shallow tip regions as discussed in U.S. Patent Application Serial No. 08/363,749, filed 12/23/94. Additionally depositing additional semiconductor material on source/drain regions enables the manufacture of "raised" source/drain regions which reduce resistances of the device and improves performance. Silicide 336 is then subsequently formed on the deposited semiconductor material 400 as shown in Figure 4B. In such a case, the deposited semiconductor material 400 combines with the previously deposited polysilicon layer 320 to set the gate electrode height (T_g). In such a case, sacrificial layer 322 should be made sufficiently thick to compensate for the additional volume occupied by the deposited semiconductor material 400.

It is to be appreciated that an advantage of the present method of confining silicide onto an electrode is the fact that it enables thin sidewall spacers (less than 300Å wide) to be used. In prior art processes, spacers having a width of at least 2000Å were required to ensure that they provided a sufficient gap or distance to prevent silicide encroachment. The use of thin

spacers to confine silicide enables the further scaling of semiconductor devices. Additionally thin sidewall spacers allow solid source diffusion to be used to form ultra shallow tip regions since dopants have only a short distance (less than 300Å) to diffuse underneath the gate electrode. Low resistance ultra shallow tips allow the fabrication of high performance semiconductor devices.

Thus, device structures and methods for preventing silicide encroachment have been described.

IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

an electrode having a first thickness;

a silicide layer on said electrode, said silicide layer having a second thickness; and

a sidewall spacer adjacent to said electrode, wherein said sidewall spacer has a height greater than the sum of said first thickness and said second thickness.

2. A metal oxide semiconductor device comprising:

a gate electrode having a first thickness;

a silicide layer on said gate electrode, said silicide layer having a second thickness;

a pair of sidewall spacers on opposite sides of said gate electrode, said sidewall spacers having a height which is greater than the sum of said first thickness and said second thickness; and

a pair of source/drain regions formed on opposite sides of said gate electrode.

3. The semiconductor device of claim 2 wherein said gate electrode comprises polysilicon.

4. The semiconductor device of claim 2 wherein said gate electrode further comprises selectively deposited semiconductor on said polysilicon layer.

5. A semiconductor device comprising:

a gate electrode formed on a gate dielectric layer formed on a first surface of a substrate;

a pair of source/drain regions formed on opposite sides of said gate electrode;

an isolation region having a top surface extending less than 1500Å above said first substrate surface; and

a silicide layer formed on said source/drain regions wherein said silicide layer has a top surface with a height less than said top surface of said isolation region.

6. The semiconductor device of claim 5 further comprising:

a gate silicide layer having a first thickness formed on said gate electrode, said gate electrode having a second thickness; and

a pair of sidewall spacers formed on opposite sides of said gate electrode, wherein said sidewall spacers have a height which is greater than the sum of said first thickness and said second thickness.

7. A method of forming a semiconductor device comprising the steps of:

forming an electrode having a first thickness;

forming a silicide layer having a second thickness on said electrode; and

forming a sidewall spacer adjacent to said gate electrode wherein said sidewall spacer has a height which is greater than the sum of said first thickness and said second thickness.

8. A method of forming an MOS transistor comprising the steps of:

forming a gate electrode on a gate dielectric layer formed on a first surface of a substrate;

forming a pair of source/drain regions on opposite sides of said gate electrode;

forming an isolation region having a top surface extending less than 1500Å above said first substrate surface; and

forming a silicide layer on said pair of source/drain regions wherein said silicide layer has a top surface with a height less than the top surface of said isolation region.

9. The method of claim 8 further comprising the steps of:

forming a gate silicide layer having a first thickness on said gate electrode, wherein said gate electrode has a second thickness; and

forming a pair of sidewall spacers on opposite sides of said gate electrode, wherein said sidewall spacers have a height which is greater than the sum of said first thickness and said second thickness.

10. A method of forming a semiconductor device, said method comprising the steps of:

forming a gate dielectric layer on a silicon substrate;

forming a silicon layer over said gate dielectric layer said silicon layer having a first thickness;

forming a sacrificial layer over said silicon layer;

patterning said silicon layer and said sacrificial layer into an electrode;

forming a pair of spacers on opposite sides of said electrode said spacers having a first height;

removing said sacrificial layer from over said silicon layer; and

forming a silicide having a second thickness on said silicon layer and on said substrate adjacent to the outside edges of said spacers, wherein said first height is greater than the sum of said first thickness and said second thickness.

11. The method of claim 10 wherein said sacrificial layer is silicon germanium.

12. The method of claim 10 wherein said spacers comprise silicon nitride.

13. The method of claim 10 wherein said sacrificial layer comprises silicon dioxide.

14. The method of claim 13 wherein said silicon dioxide layer is doped with fluorine.

15. The method of claim 10 wherein said sacrificial layer is removed with a wet etchant.

16. The method of claim 10 further comprising the step of:

polishing said silicon layer prior to forming said sacrificial layer.

17. The method of claim 10 further comprising the step of:

doping said silicon layer after removing said sacrificial layer.

18. The method of claim 10 wherein said step of forming said silicide layer comprises the steps of:

blanket depositing a refractory metal over said substrate, said pair of sidewall spacers, and said silicon layer;

thermally reacting said refractory metal with said substrate and said silicon layer to form a refractory metal silicide; and

removing said refractory metal from said pair of spacers.

19. The method of claim 10 wherein said step of forming said silicide layer comprises the step of:

selectively depositing said silicide layer on said silicon layer and on said substrate.

20. The method of claim 10 wherein said spacers have a height greater than the sum of the thickness of said silicon layer and said silicide layer.

21. The method of claim 10 wherein said silicon layer is polycrystalline silicon.

22. The method of claim 10 wherein said spacer height is greater than the sum of said silicon thickness plus said gate dielectric thickness.

23. A method of forming a device, said method comprising the steps of:

forming a silicon electrode having a first thickness;

forming a metal layer on said silicon electrode; and

forming a silicide on said silicon electrode by reacting said metal layer and said silicon gate electrode, wherein said silicide has a second thickness, said second thickness at least twice said first thickness.

24. A method of forming a semiconductor device in a semiconductor substrate comprising the steps of:

forming an isolation region in said semiconductor substrate;

etching said semiconductor substrate adjacent to said isolation region to form a recess region; and

forming a silicide in said recessed region.

25. A method of forming an integrated circuit comprising the steps of:

forming an isolation region in a semiconductor substrate, said isolation region having a top surface extending less than 1500Å above said semiconductor substrate;

forming a first and second diffusion region adjacent to and on opposite sides of said isolation region in said semiconductor substrate; and

forming silicide on said first and second diffusion regions wherein said silicide has a top surface with a height less than the top surface of said isolation region.

26. A method of forming a semiconductor device, said method comprising the steps of:

forming a silicon film above a substrate;

forming a silicon germanium film on said silicon film;

patterning said silicon film and said silicon germanium film into an intermediate electrode;

forming a pair of sidewall spacers on opposite sides of said intermediate electrode;

removing said silicon germanium film from said intermediate electrode to reveal said silicon film; and

forming a silicide film on said silicon film.

27. The method of claim 26 wherein said silicon film is polycrystalline silicon.

28. The method of claim 26 wherein said silicon germanium film is removed with a mixture of NH_4OH and H_2O_2.

29. The method of claim 26 wherein said silicon germanium film is removed with sulfuric acid (H_2SO_4).

ABSTRACT OF THE INVENTION

A semiconductor device having a novel spacer structure and method of fabrication. The present invention describes a semiconductor device which has an electrode with a first thickness. A silicide layer having a second thickness is formed on the electrode. A sidewall spacer which is formed adjacent to the electrode has a height which is greater than the sum of the thickness of the electrode and the thickness of the silicide layer.

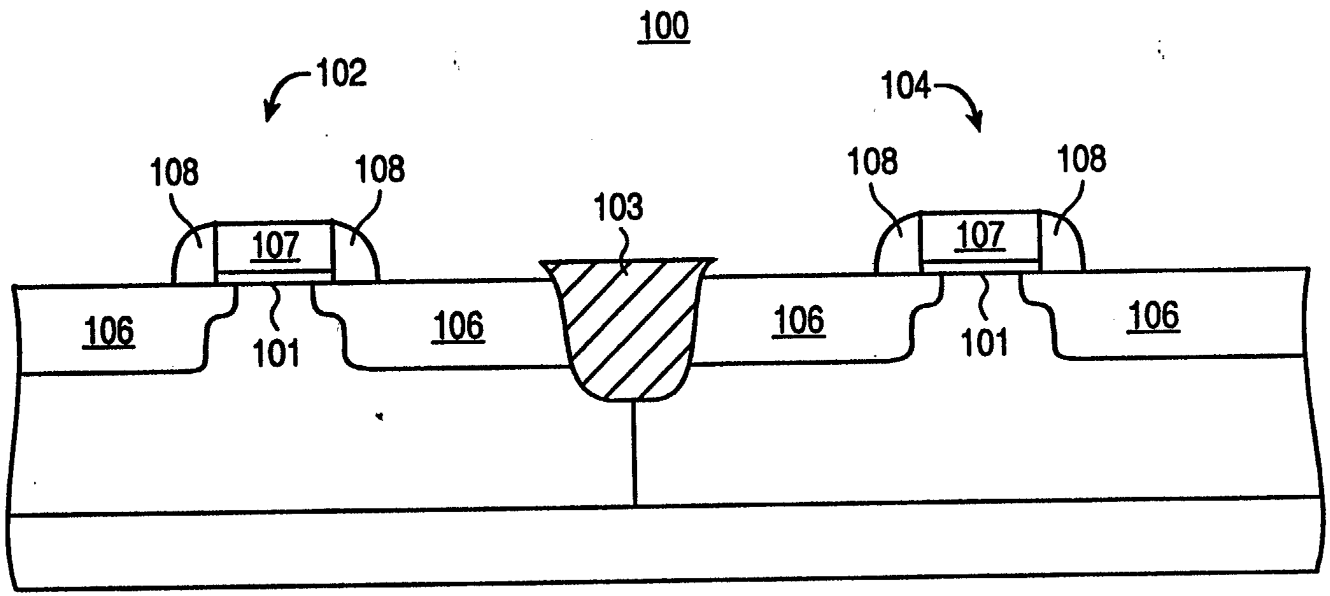

FIG. 1A

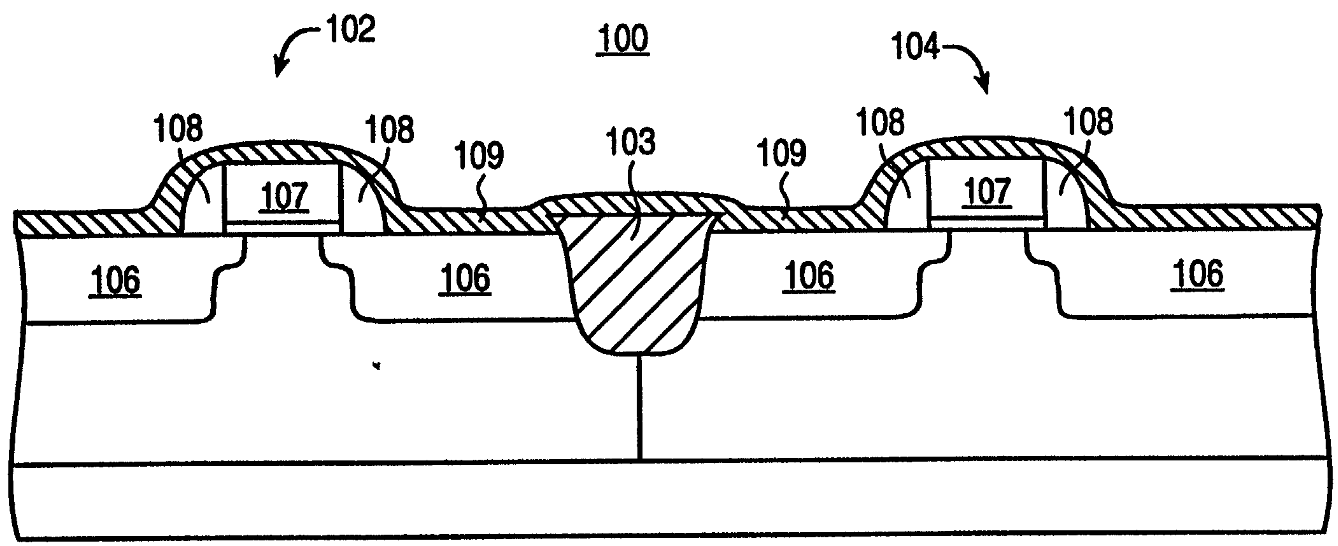

FIG. 1B

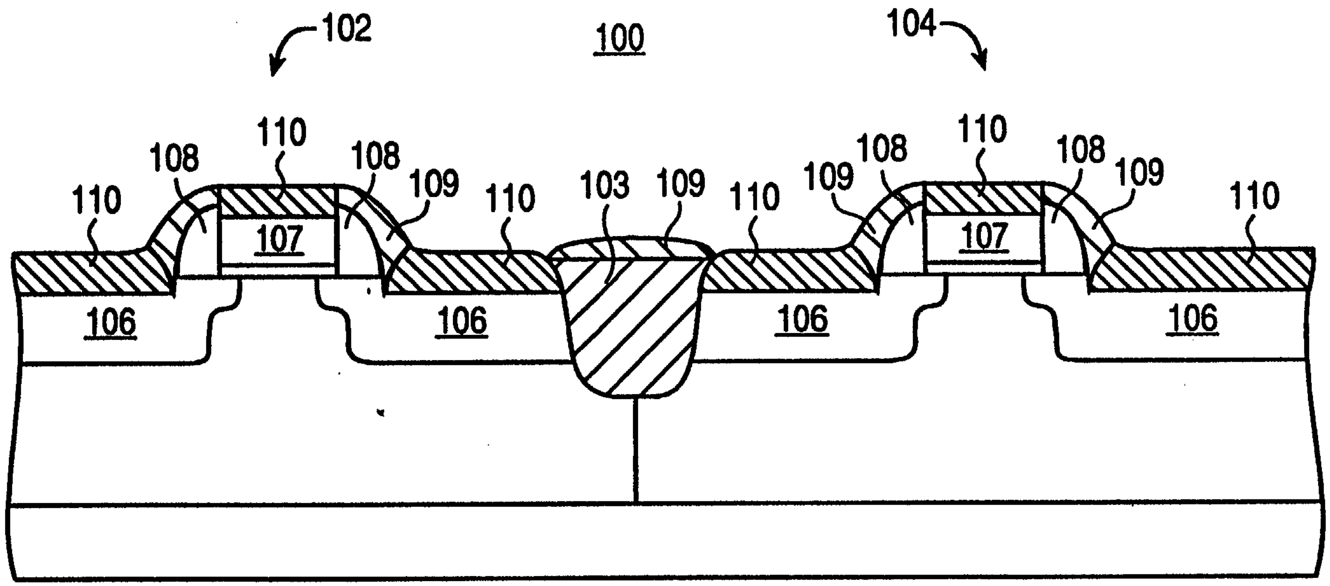

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FIG. 1C

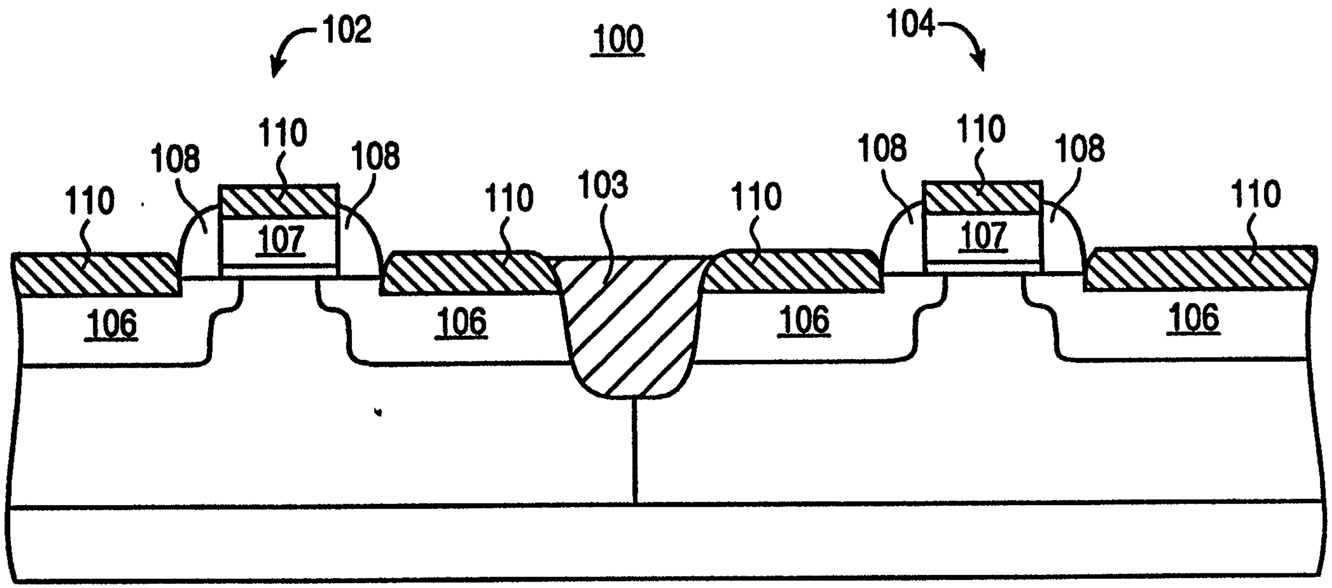
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FIG. 1D

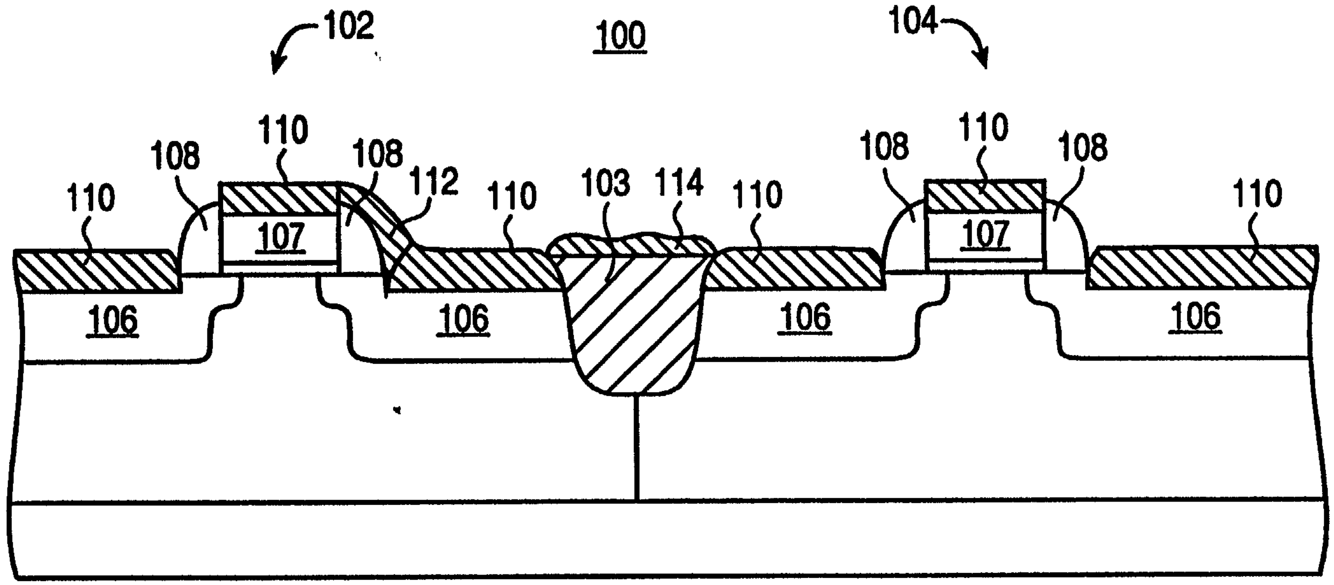

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FIG. 1E

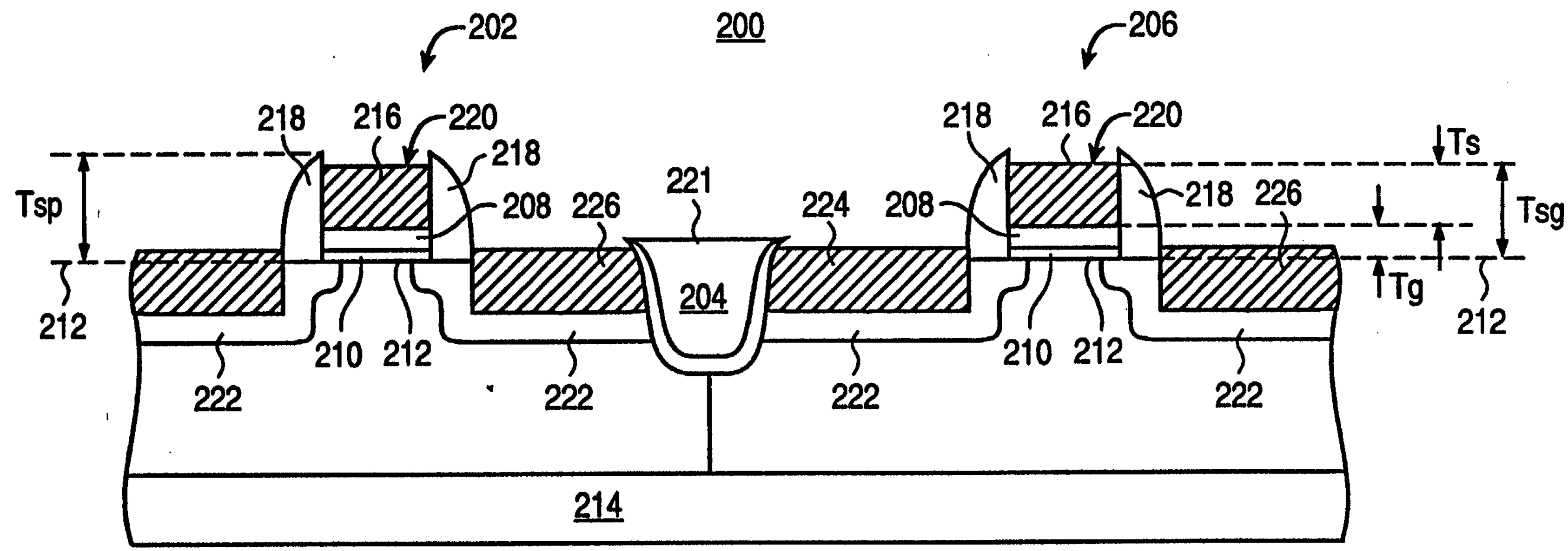
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FIG. 2

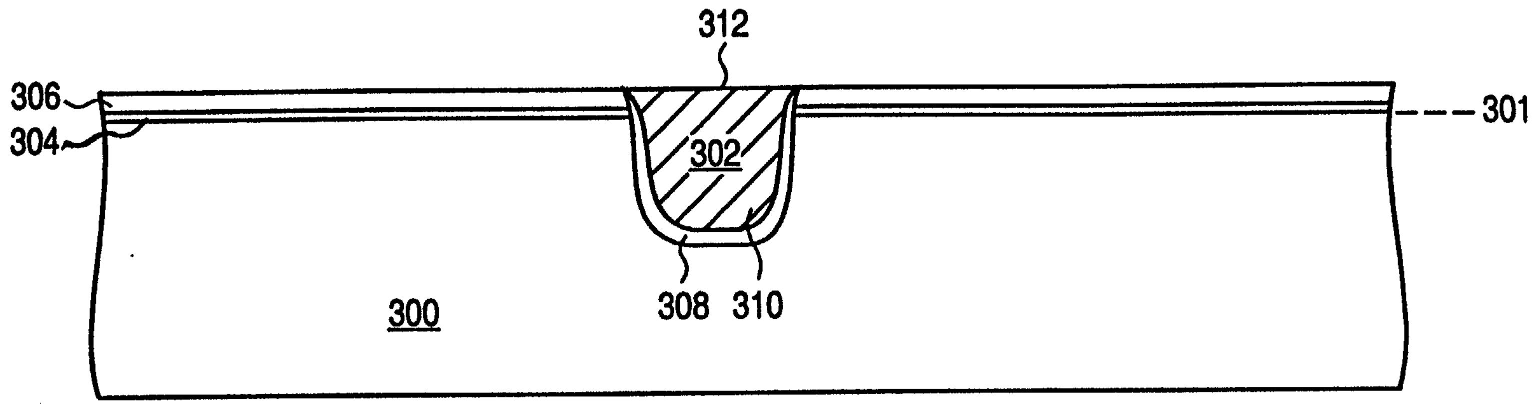

FIG. 3A

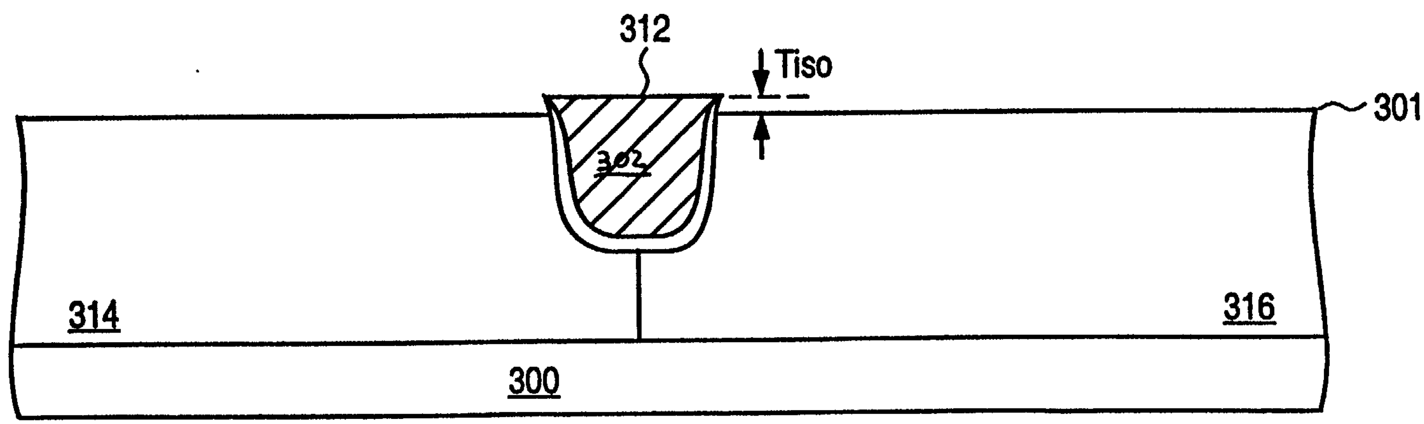

FIG. 3B

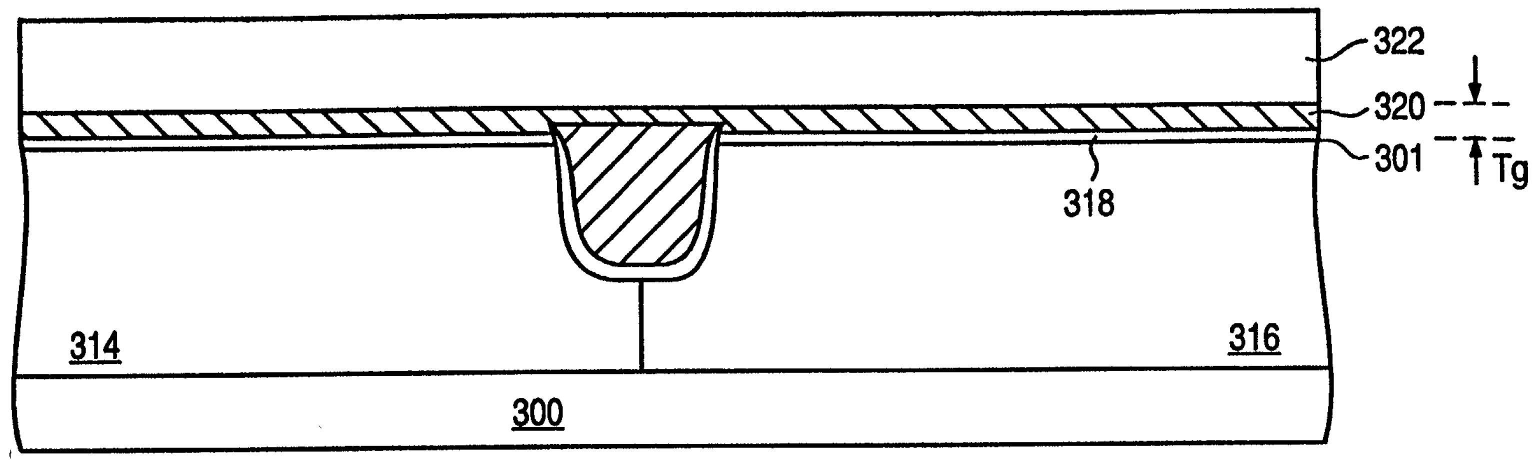
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FIG. 3C

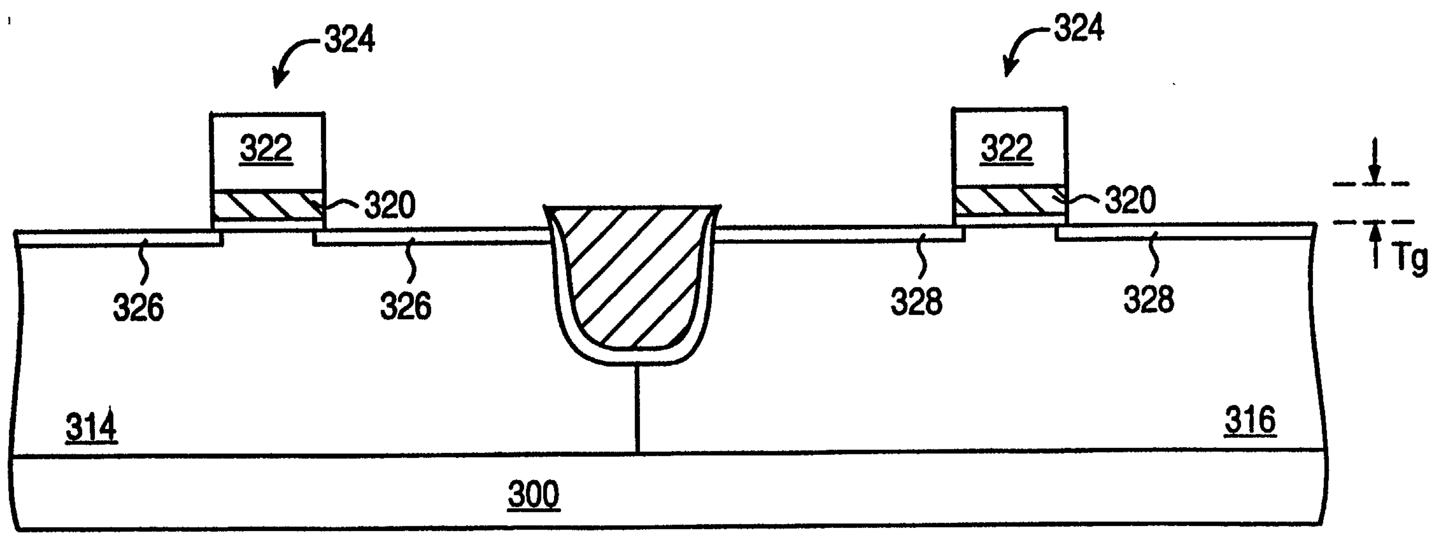
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FIG. 3D

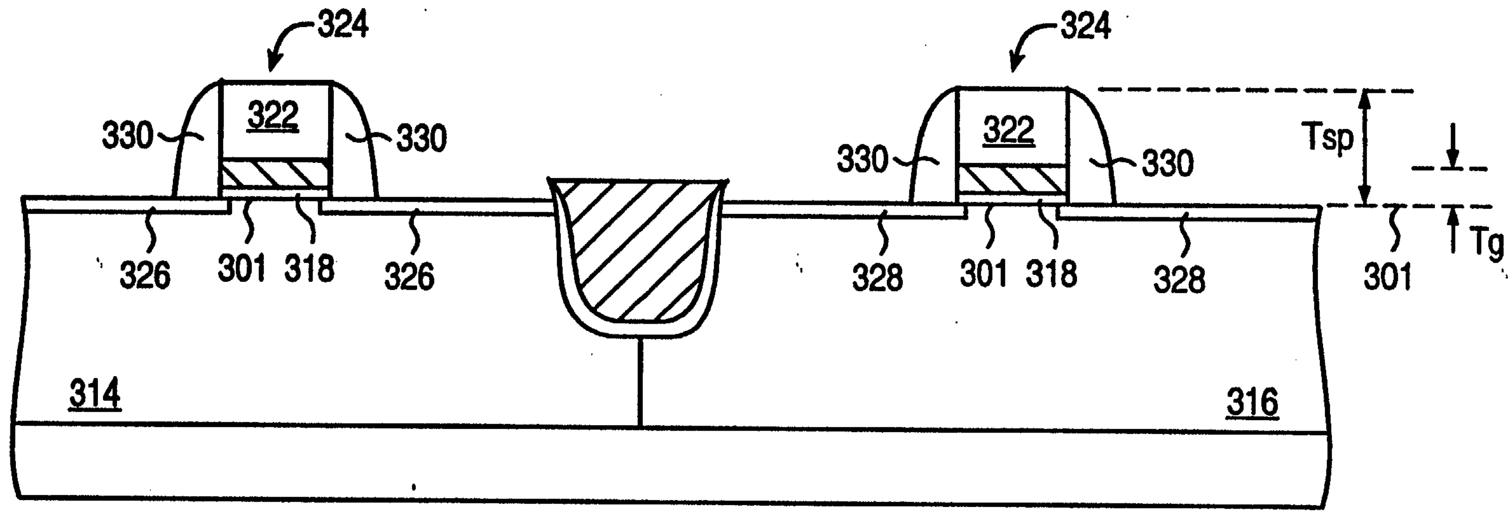
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FIG. 3E

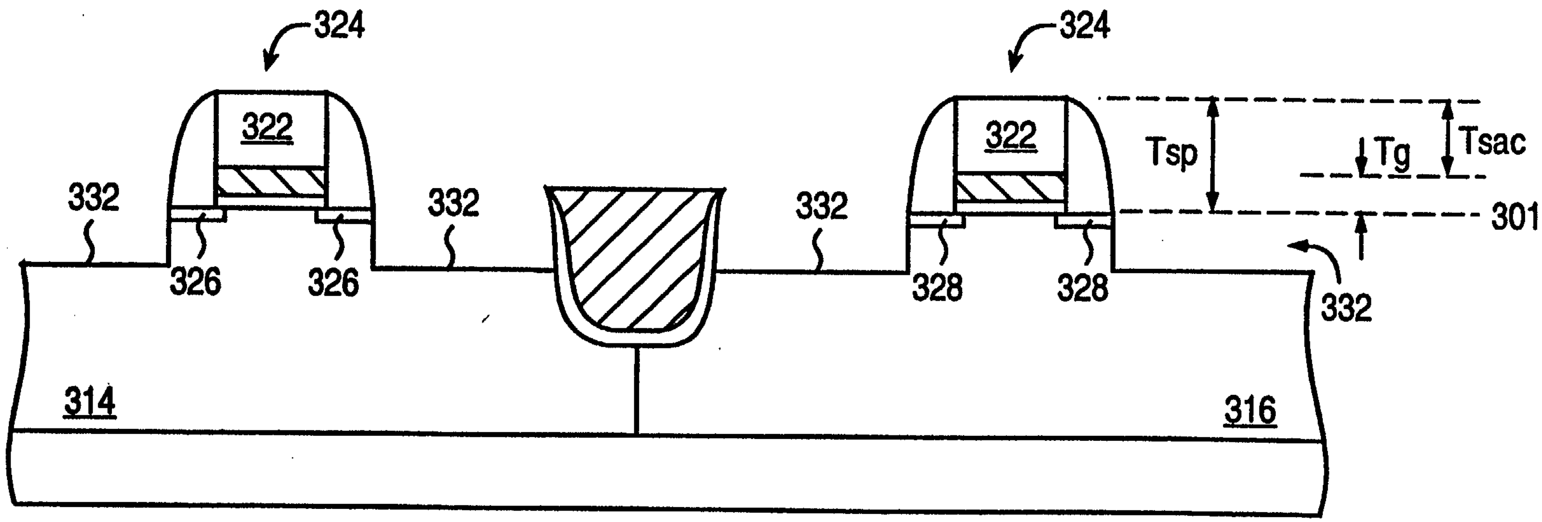
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FIG. 3F

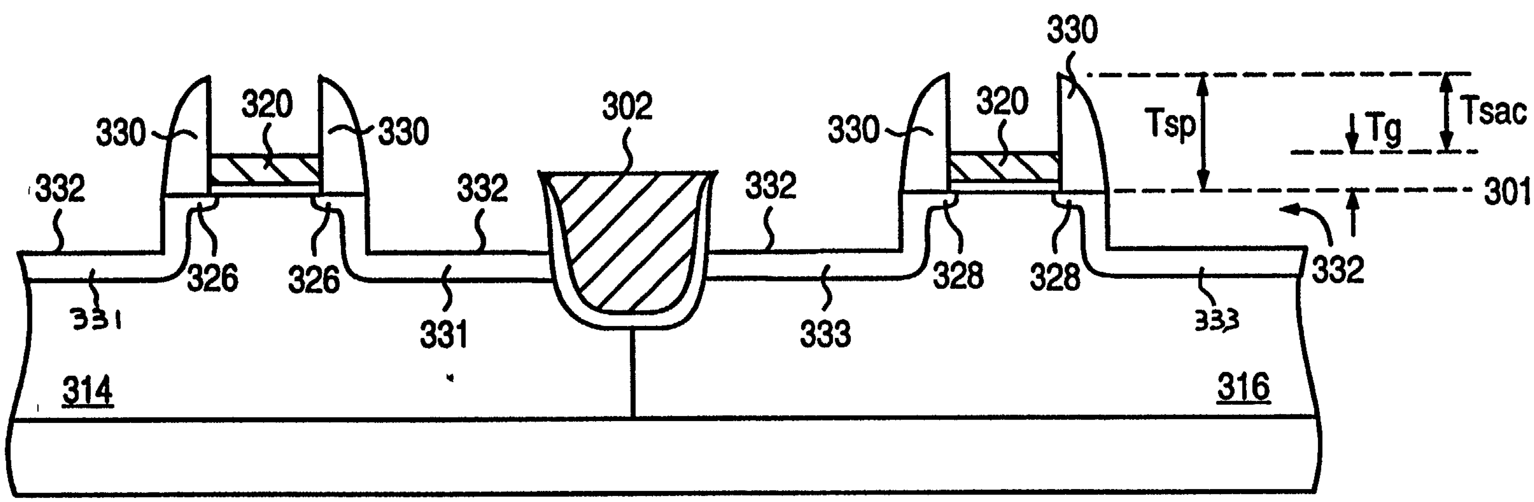
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FIG. 3G

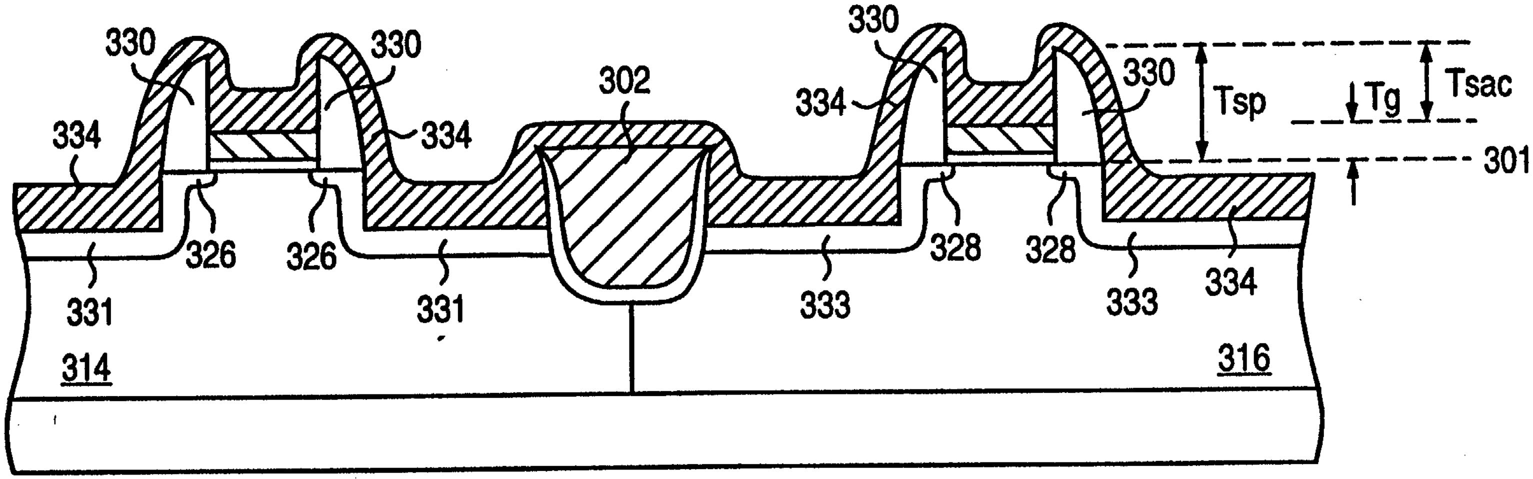
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FIG. 3H

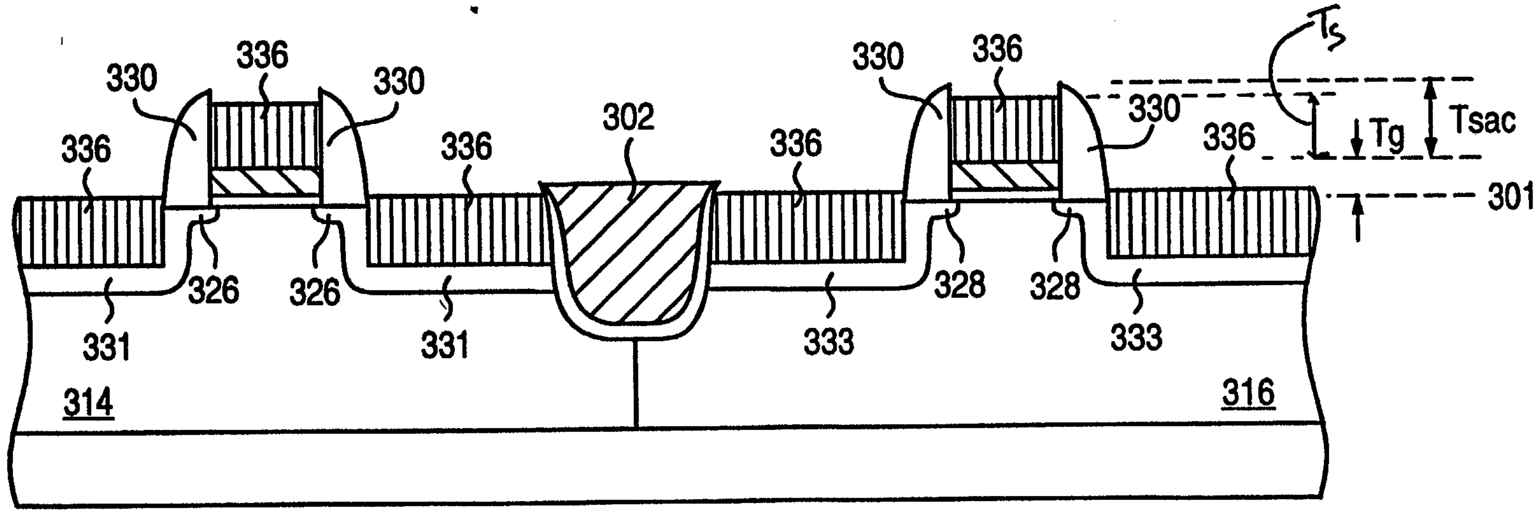
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FIG. 3I

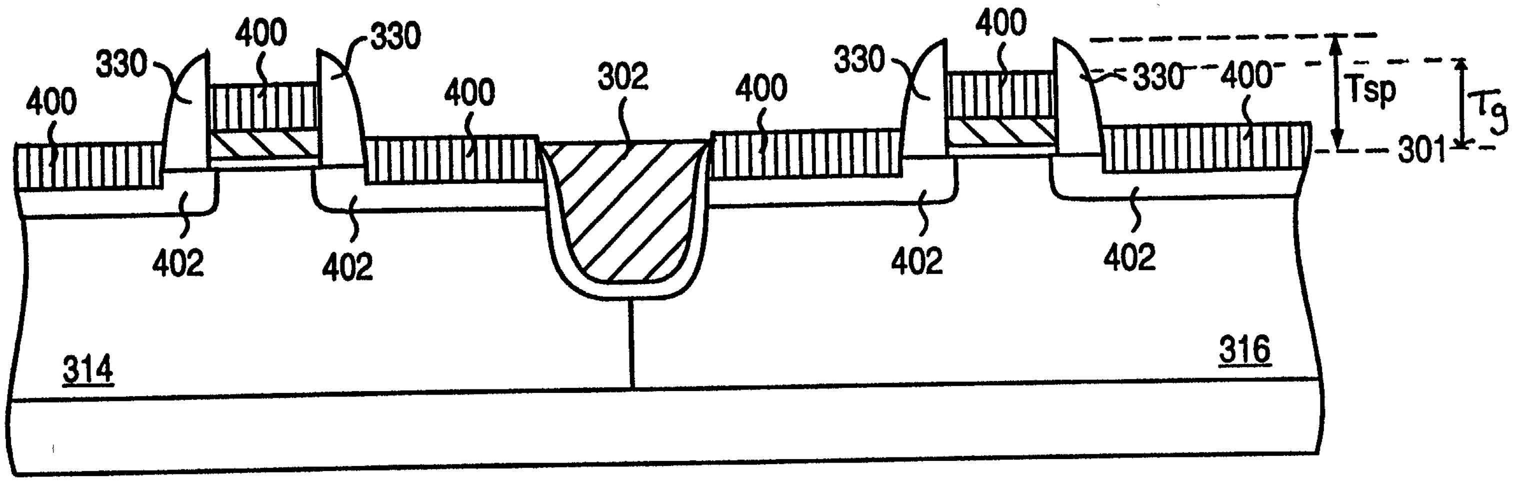
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FIG. 4A

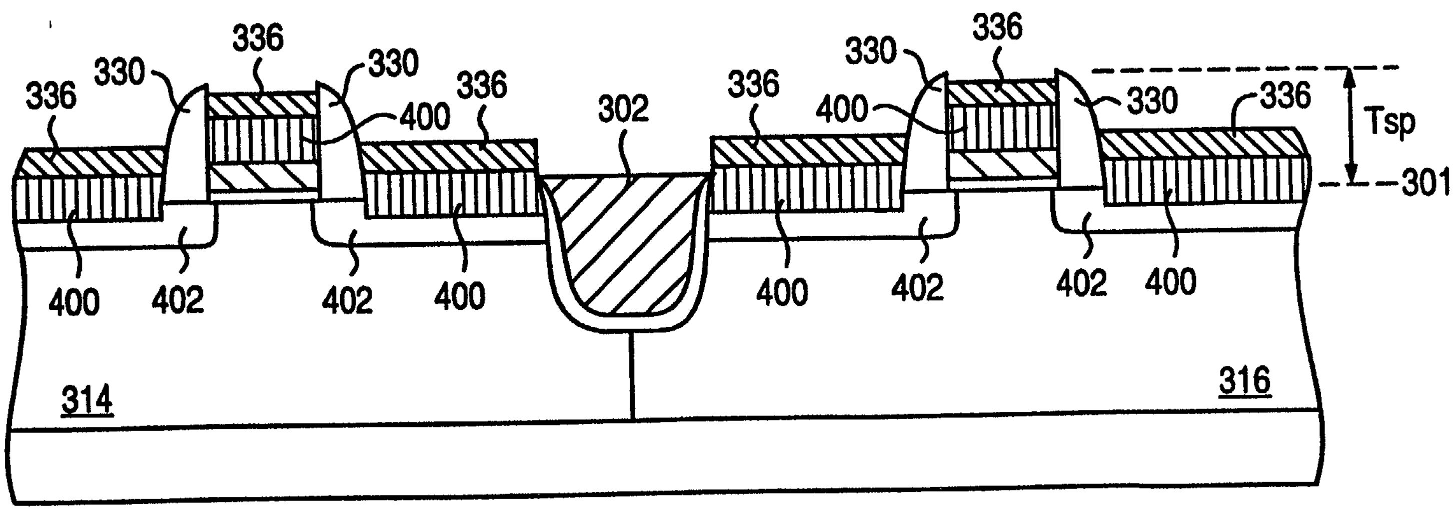
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FIG. 4B

Attorney's Docket No.: 042390.P4222 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DEVICE STRUCTURE AND METHOD FOR REDUCING SILICIDE ENCROACHMENT

the specification of which

________ is attached hereto.
XX was filed on June 30, 1997 as
United States Application Number 08/884,912
or PCT International Application Number____________
and was amended on ________________________.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.